Objective:

The objective of this lab was to build a 32 location by 8 bit contents RAM using 4 16x4 RAMs. The desired address and data were specified with DIP switches. With the toggle switch, the read or write action was selected for the RAM, which means when the toggle is high, it is reading and when the toggle is low, it is writing. The data of current address was displayed at all times. The format of the DIP switch input was the Interleaved and Sequential address memories.

Components:

- 2 –Hex-Inverter 74LS04
- 4 –7489 RAM Chips
- 2 –Octal Buffer
- 2– 74LS247 BCD to 7- Segment Decoder
- 2 –Switches
- 2 –220Ω Resistors
- 1 –5V DC Power Supply

Experimental Approach:

To make a 32 location by 8-bit contents RAM, we need 4 16x4 RAMS. There are 8 input byte D0-D7 and 5 input addresses. Also there is a control bit for write/read mode. The total inputs are 8+5+1=14.

BYTE 0	BYTE 1
X X X A_4 A_3 A_2 A_1 A_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 are the in the input values. A_3 A_2 A_1 A_0 are the in input addresses, A_4 is the control bit of low and high address location. RAM 7489 can store any 8 bits numbers input and save in any 32 location address.

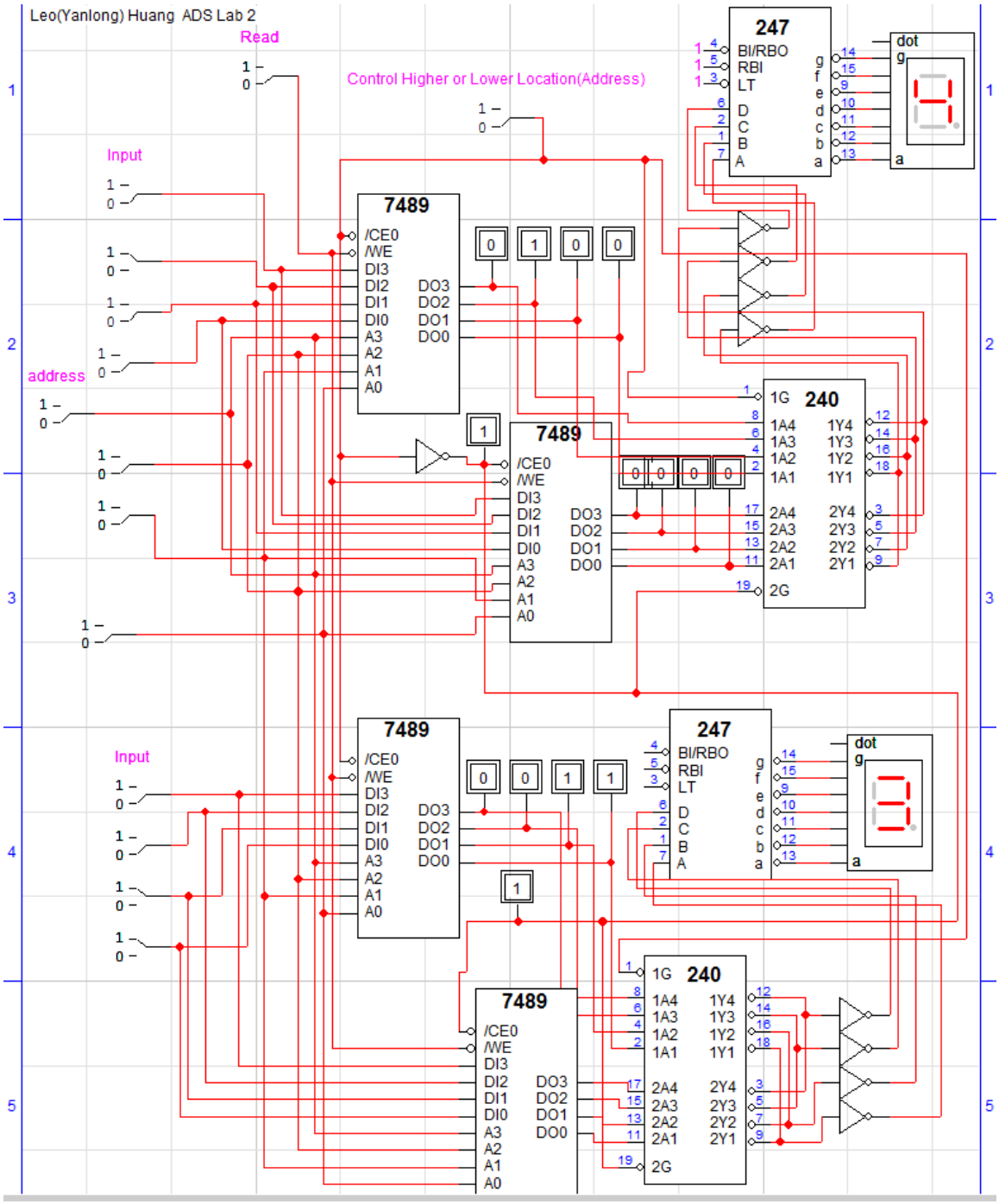
For example, in the write mode condition, the input of BYTE 1 is 0011 0010 and BYTE 0 is 0 1111. That means RAM will store number 32 (binary 0011 0010) in the low address 15(binary 1111). If the input is changed to read mode, RAM can read the number 32 (binary 0011 0010) from the address 15(binary 1111).

Example Graph

ADDRESS(LOW)	ADDRESS(HIGH)	ADDRESS(LOW)	ADDRESS(HIGH)
0	16	0	16
1	17	1	17
2	18	2	18
3	19	3	19
…..	…..	…..	…..
14	30	14	30
(0011) 15	31	(0010) 15	31

The octal buffer is require in our schematic because there are 4 RAM chips that means there are 16 output but we have only 8 input for the LED light display. Two inputs cannot combine as one input for each A, B, C, D input. The digital buffer can isolate the input from the output, preventing the impedance of one circuit from altering the impedance of another. It can hold one input and output another input which is really useful in this lab.

Circuit Schematic:



Result:

The 32 location by 8 bit contents RAM using 4 16x4 RAMs was designed and the desired address and data were specified with DIP switches. With the toggle switch, the read or write action was selected for the RAM, which means when the toggle is high, it is reading and when the toggle is low, it is writing. The data of current address was displayed at all times. In writing mode, we can input any 8 bits numbers to any 32 low or high addresses. In reading mode, we can read any 8 bits number already be stored in the 32 ram location.

Conclusion:

To conclude, we were able to complete the lab successfully. The simulation was implemented successful but we were unable to design the circuit properly which is why our circuit had some wiring error and did not work properly. Overall, our lab met all the requirements listed in the assignment.