VLSI Design Project
4-bits ripple carry adder
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1. Introduction

Assuming we need to calculate A+B and

A= A3 A2 A1 A0

B=B3 B2 B1 B0

（similar as 8 bits)

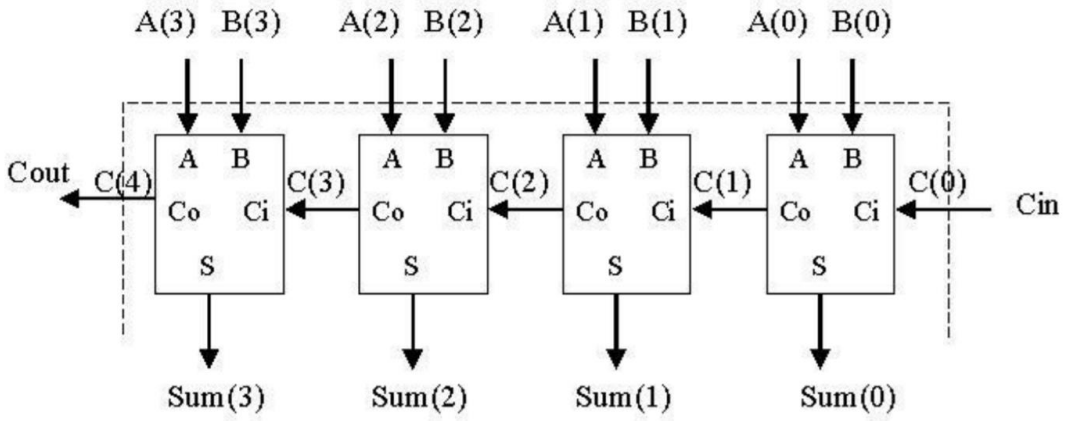
For example:

A= 1 0 1 1 +

B= 1 1 0 1

A+B= 11 0 0 0 = $C_{out}\ S_3\ S_2\ S_1\ S_0$

From the example above it can be seen that we are adding 3 bits at a time sequentially until all bits are added. A full adder is a combinational circuit that performs the arithmetic sum of three input bits: augends Ai, addend Bi and carry in Cin from the previous adder. Its results contain the sum Si and the carry out, Cout to the next stage.

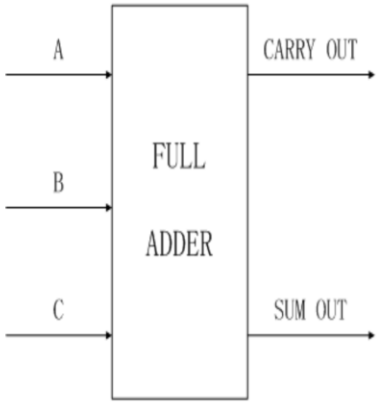


2. Personal & team-mate's contribution to the project

I finish the project by myself and ask the TA for some helps.

3. Problem Formulation

So to design a 4-bit adder circuit we start by designing the 1 –bit full adder then connecting the four 1-bit full adders to get the 4-bit adder as shown in the diagram above. For the 1-bit full adder, the design begins by drawing the Truth Table for the three input and the corresponding output SUM and CARRY. The Boolean Expression describing the binary adder circuit is then deduced. The binary full adder is a three input combinational circuit which satisfies the truth table below.



A	B	C	SUM OUT	CARRY OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig.2. Diagram and Truth Table of Full Adder

The Boolean equations of a full adder are given by:
Sout = ABC + AB'C' + A'B'C + BA'C' =(AB'+BA')C +AB+A'B') C'
Sout = A⊕B⊕C Cout = AB + AC + BC
Cout = AB + C (A⊕B)
The circuit diagram is shown in Fig.3 and the simulation results is shown in Fig. 4:

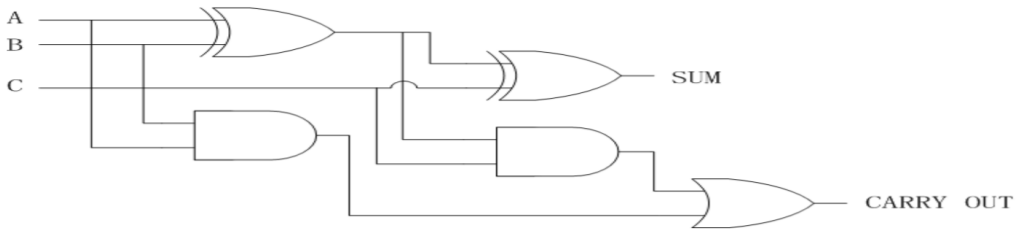


Fig. 3. The Gate level Diagram of Full Adder

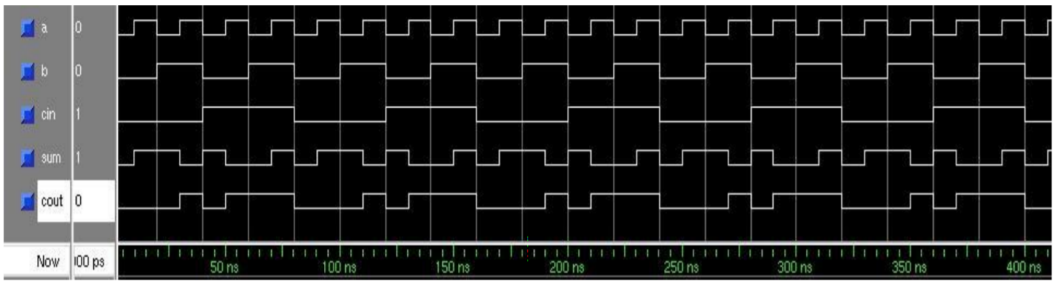


Fig. 4 1 bit full adder simulation results

As is seen from Fig. 5 and Fig. 6 the carry ripples through the 4 full adders to appear at the output, while the sums are available after 2 XOR delay.

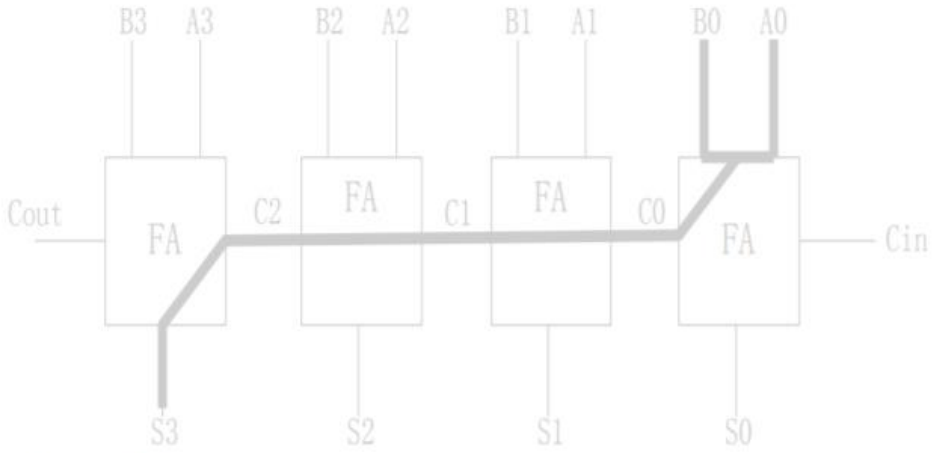


Fig. 5 Carry Propagation

The carry propagation is shown in Fig. 5 as a block and as a path through the circuit in Fig. 6

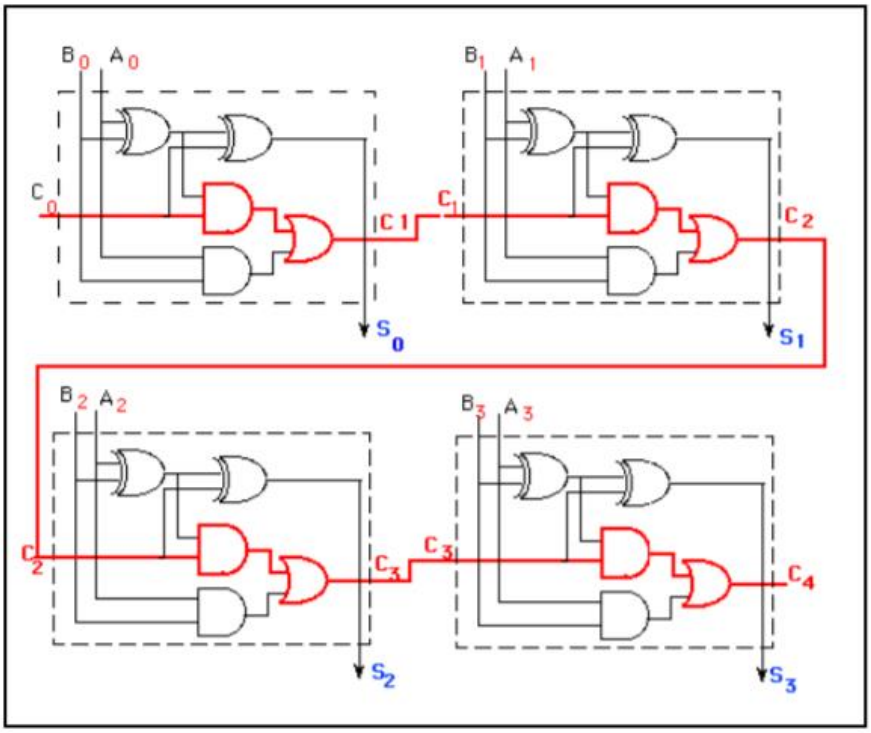


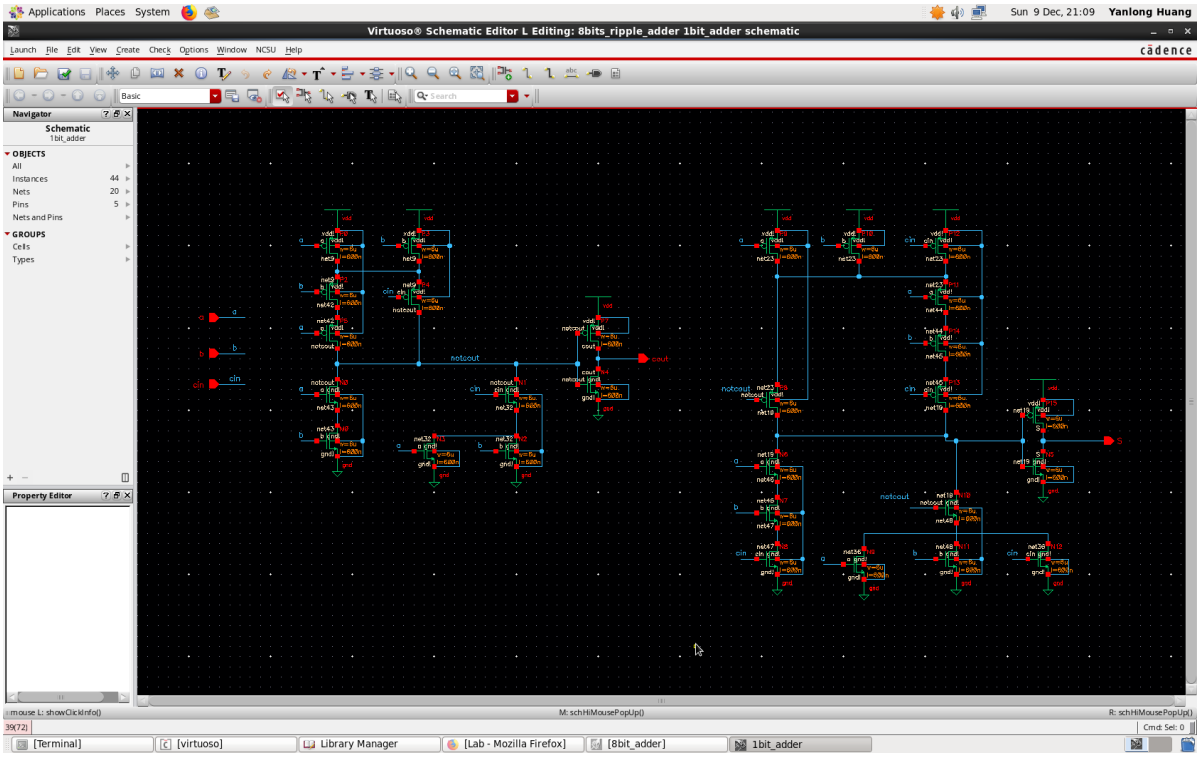
Fig. 6 carry propagation through the circuit

4. Cmos Design

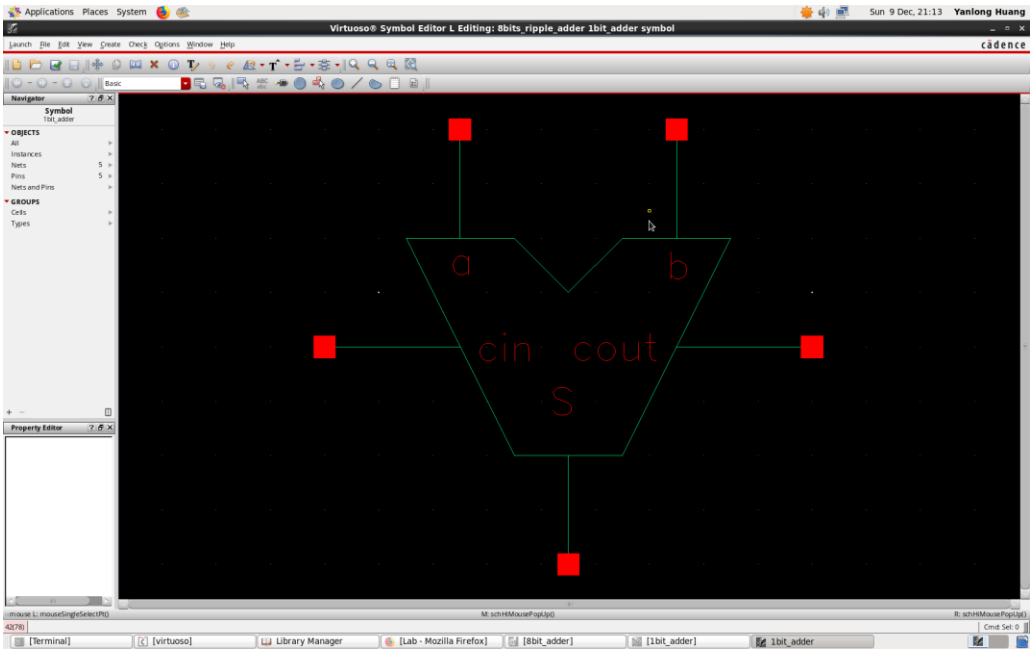
4.1 .1

1Bit adder Schematic and symbol

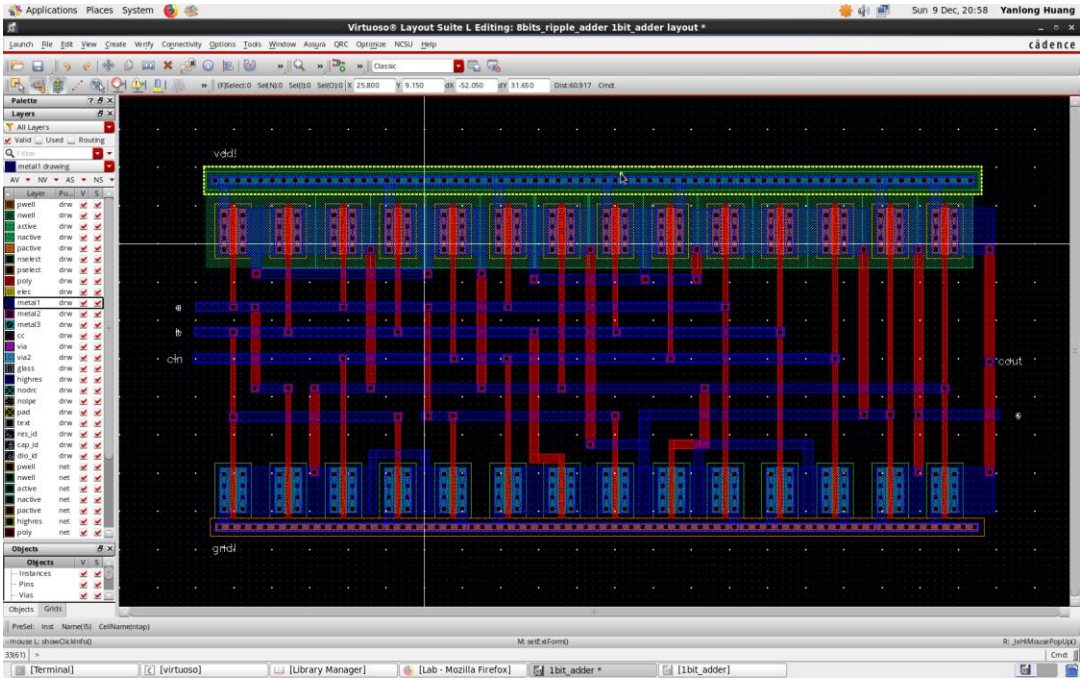
I have created the 1 bit and 8 bits carry adder schematic and layout, also run the simulation of ADE from the schematic.



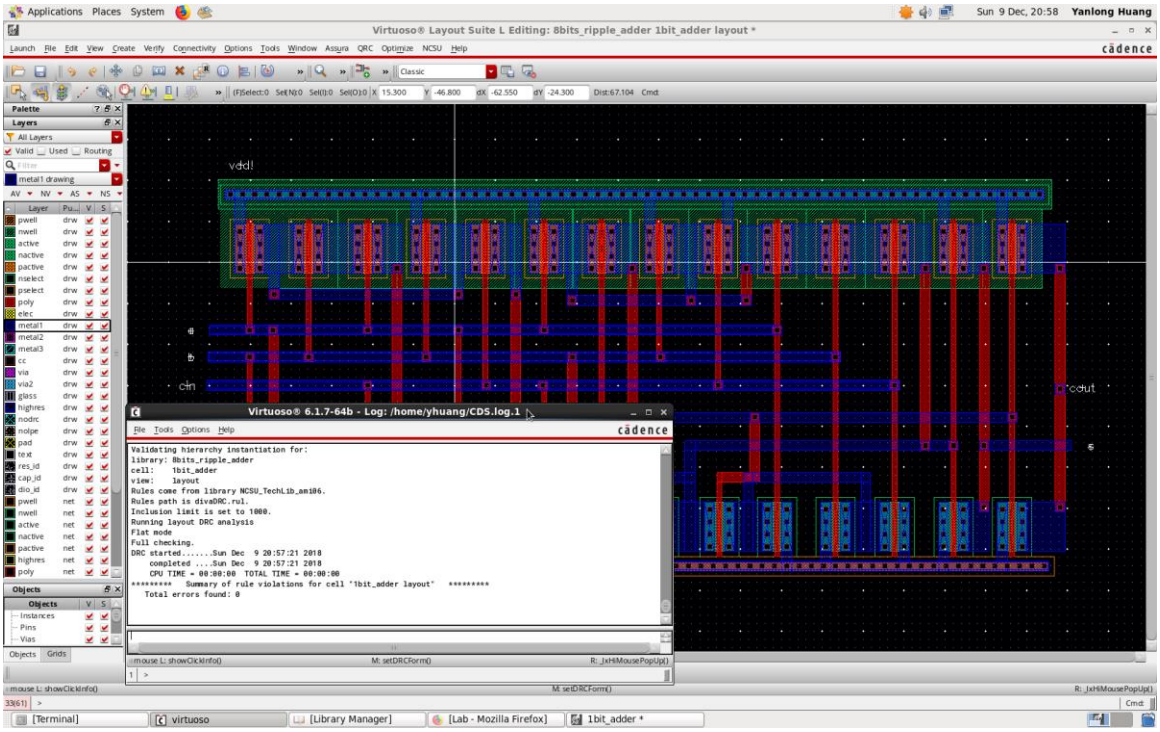
Symbol



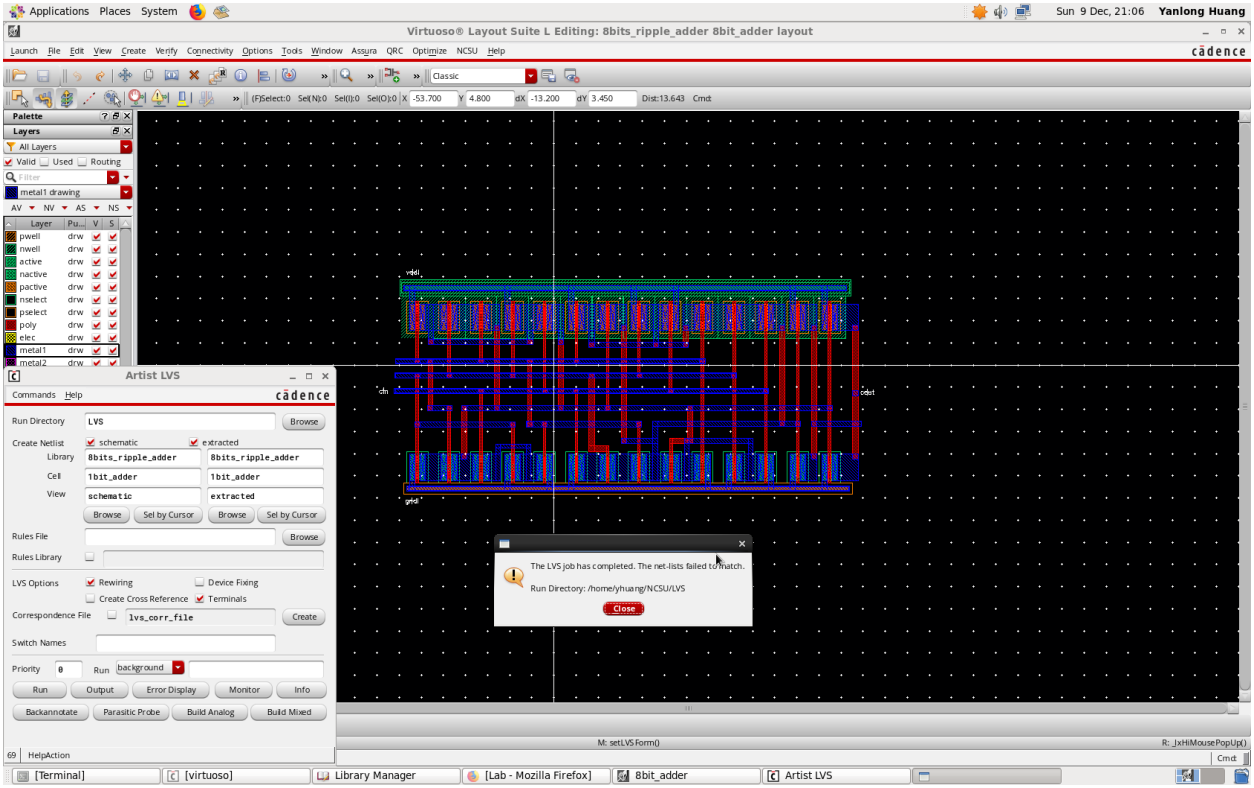
4.1.2 Layout and Extracted



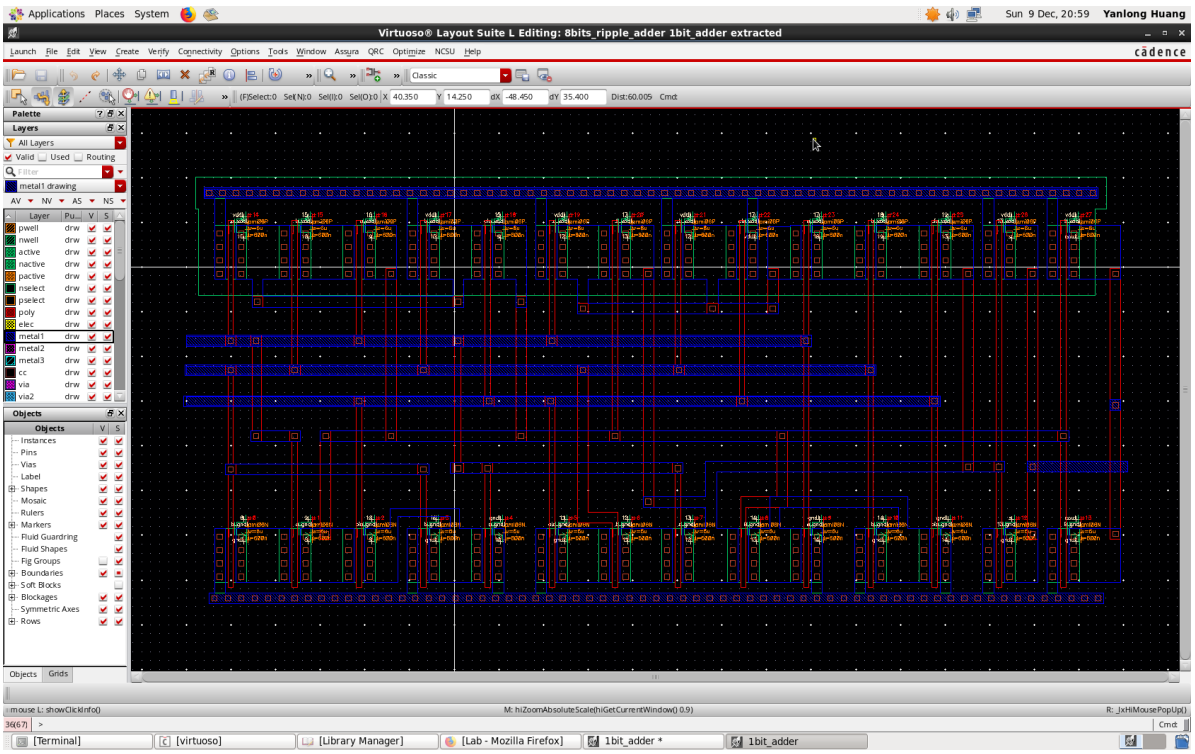
DRC Layout, no errors.



Netlist failed to match

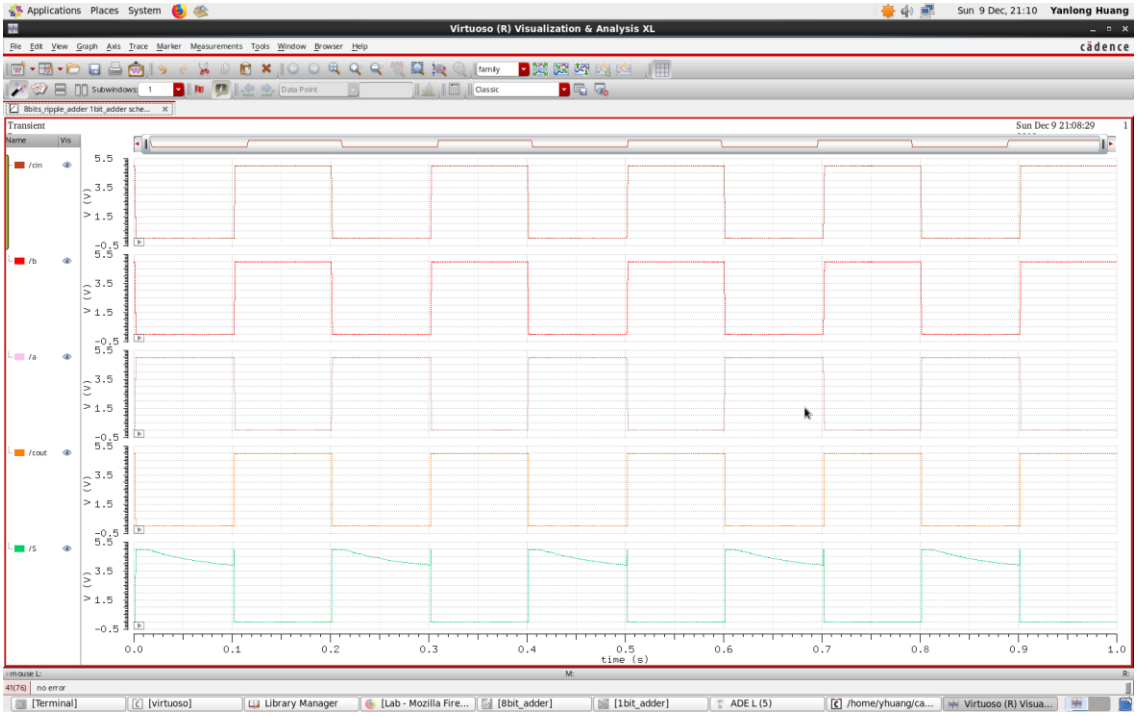


Extracted

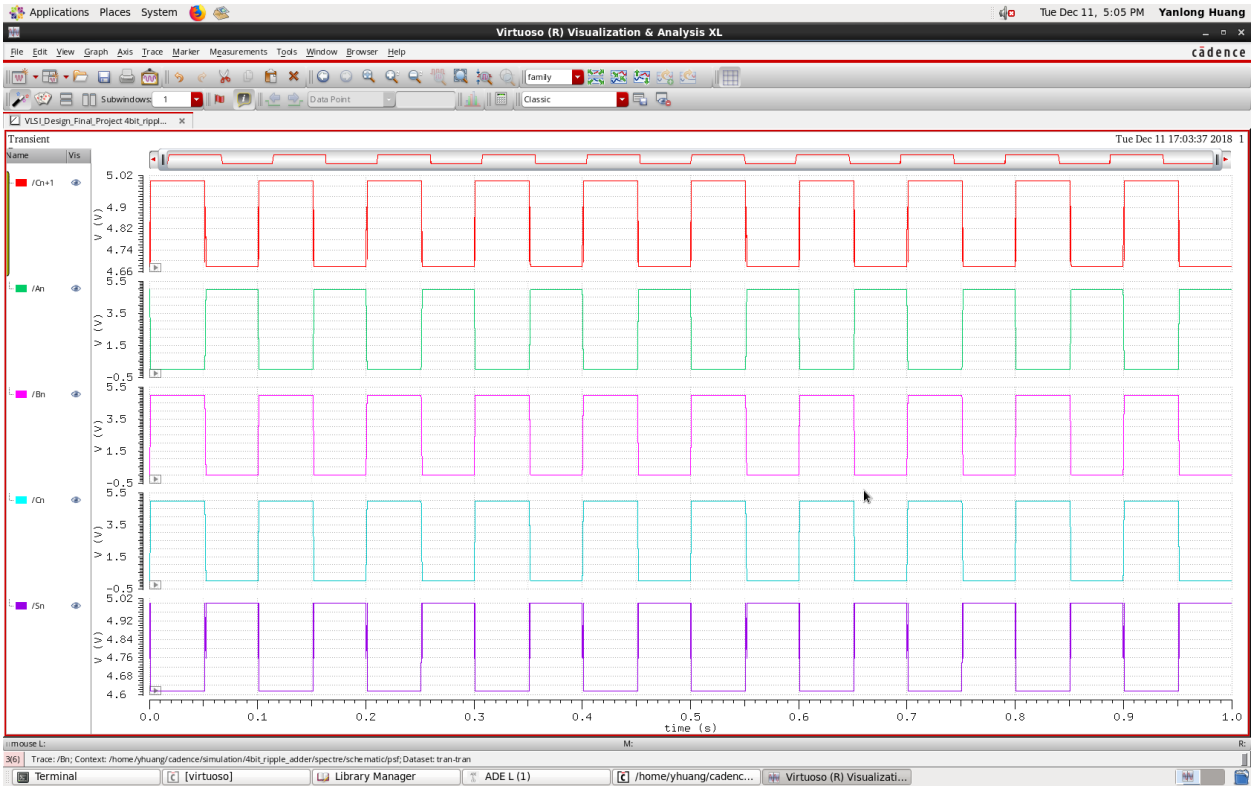


4.1.3 Simulation Result

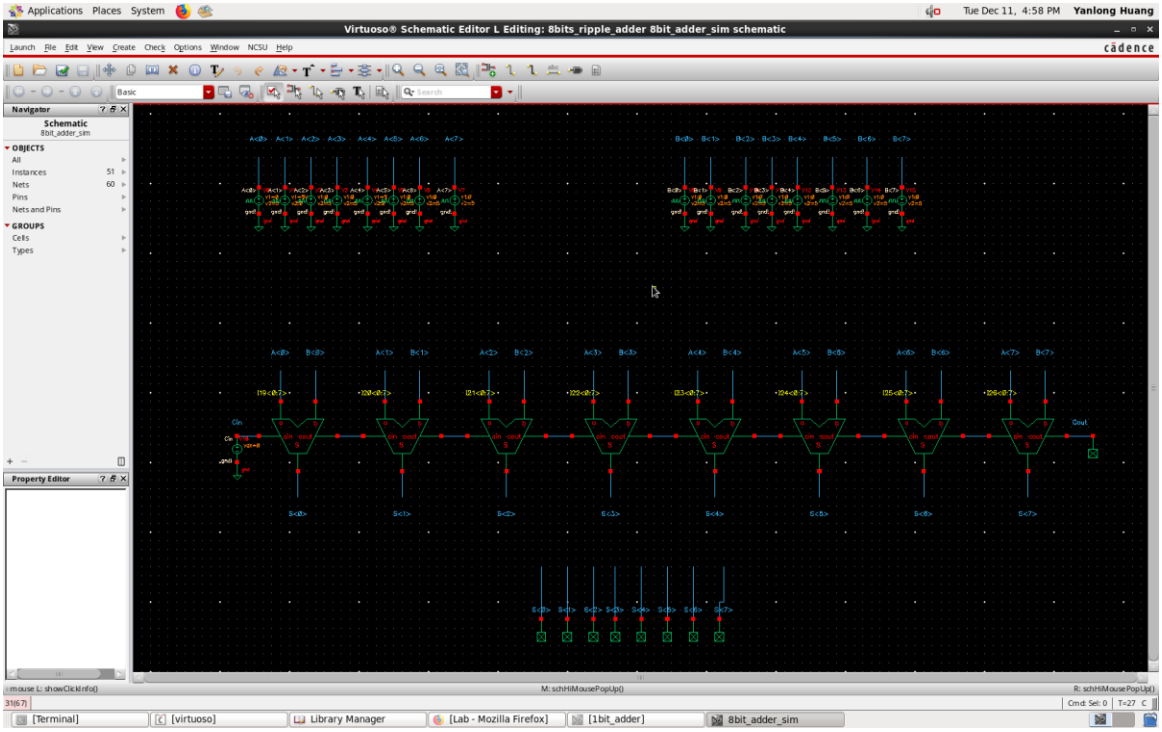
(The Cmos I use in NCSU has come problem and that caused the S output is not a prefect square. I test the same schematic in Cadence45 technology. The simulation is prefect.)



Simulation result in Cadence45 technology:

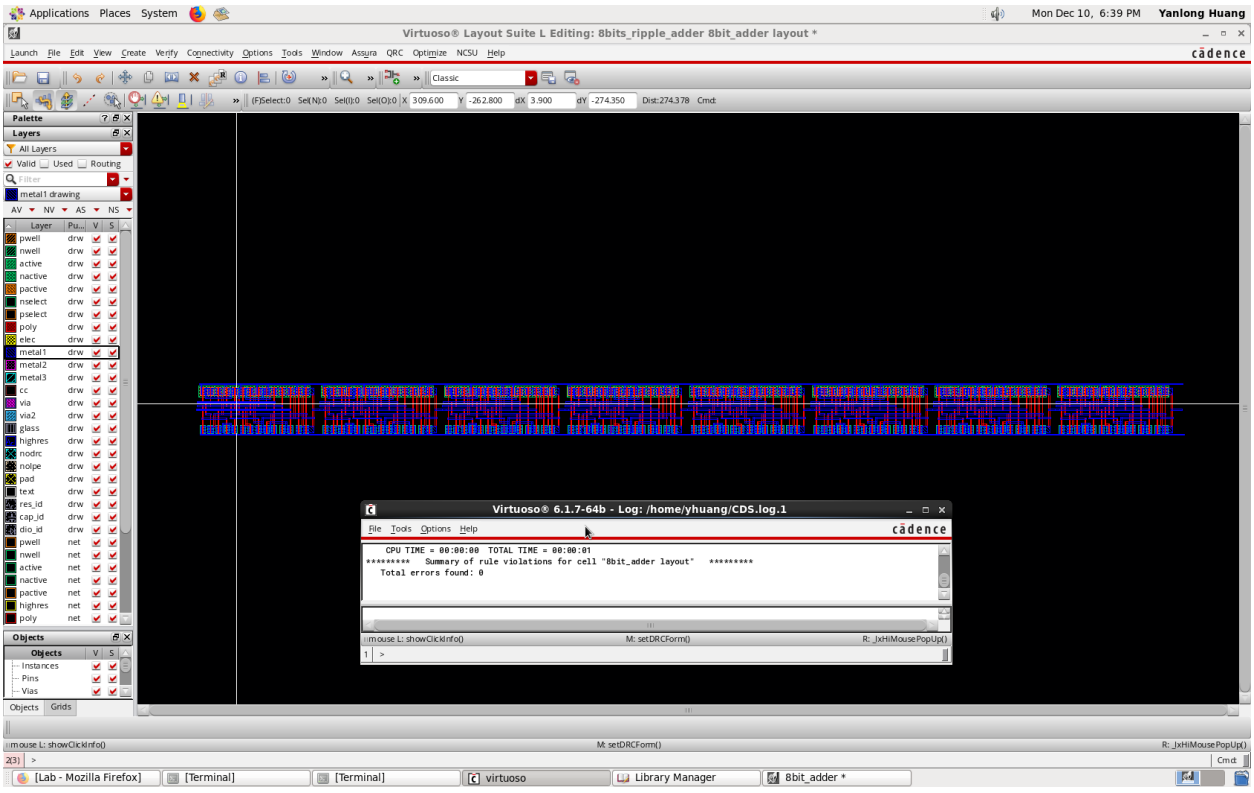


4.2.1 8-bits schematic



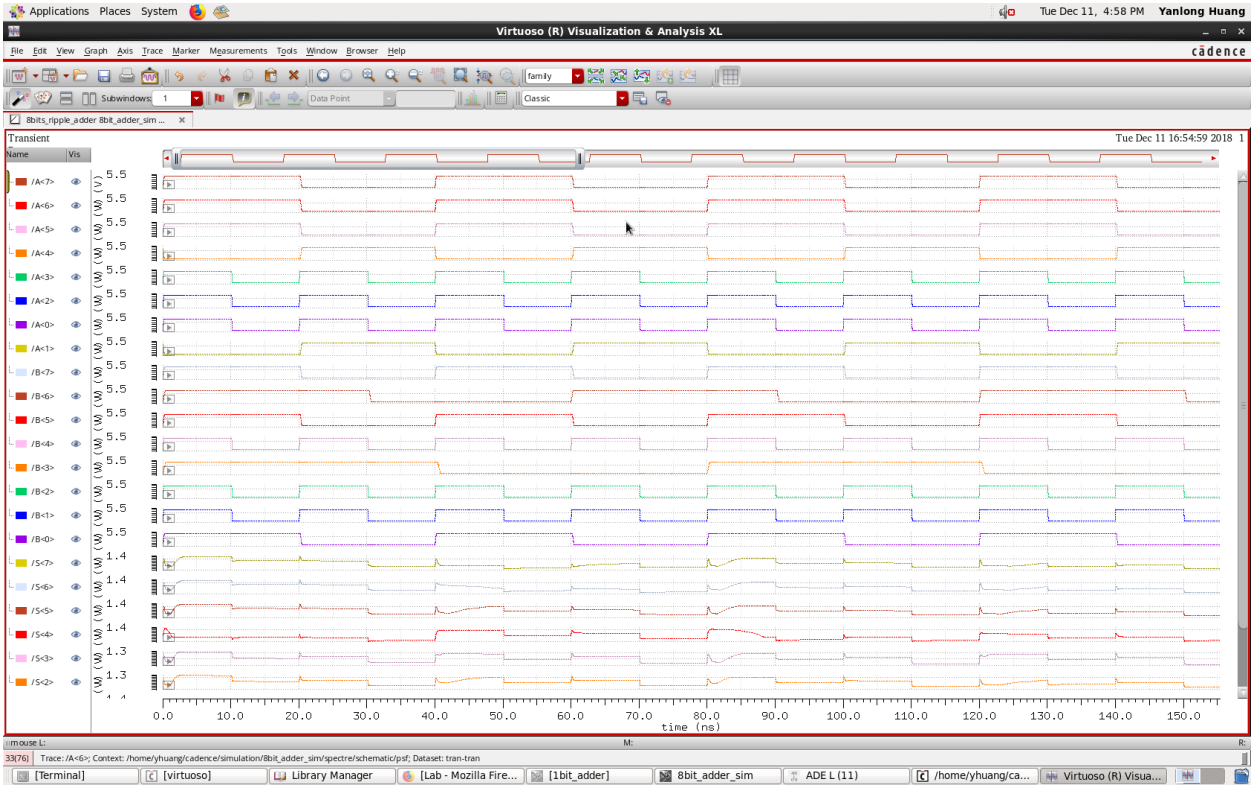
4.2.2 8-bits Layout

DRC with no errors.



4.2.3 8-bits simulation result

(In NCSU, the 1 bit adder result will affect the result in 8 bits)



5. Delay optimization

There is no delay optimization in this project.

6. Troubleshooting

After 1 bit adder schematic was built, the result of the S in the graph is not perfect. In order to find out the reason, I built the exactly same 1 bit adder circuit in Cadence45 technology and the result is prefect. That means the circuit has no errors. The reason that Sum cannot get the prefect result in NCSU is the cmos model.

7. Conclusion

I have successful build the 8 bits ripple adder schematic in Cadence NCSU, and the simulation result is correct but the square wave is not perfect (only prefect in cadence45 technology). The layout was build but the netlist match failed.

8. Reference

Cadence tutorial from CMOS.COM
http://cmosedu.com/jbaker/courses/ee421L/f14/students/ibanezv/lab7/lab7.htm